

REMARKS

This is in full and timely response to the Office Action dated August 8, 2007.

Claims 1-16 are currently pending in this application, with claims 1, 4 and 7 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Claim to priority

Item 12(a)(1) on the first page of the Office Action contends that none of the certified copies of the priority documents have been received.

In response, a review of the records found within “Public PAIR” at the website for the U.S. Patent and Trademark Office reveals the presence of a Certified Copy of Foreign Priority Application having a filing date of January 24, 2003.

An acknowledgement of the claim to foreign priority under 35 U.S.C. §119 is respectfully requested.

New non-final Office Action

If the allowance of the claims is not forthcoming at the very least and a new ground of rejection made against any of claims 1-6, then a **new non-final Office Action** is respectfully requested at least for the following reasons.

Rejection under 35 U.S.C. §112

Paragraph 2 of the Office Action indicates that claim 4 has been rejected under 35 U.S.C. §112, second paragraph.

This rejection is traversed at least for the following reasons.

Claim 4 - Claim 4 is drawn to a display device used as a display part of an electronic device capable of switching between a normal power consumption state and a low power consumption state, operating according to display data and power supply voltage supplied from a side of the electronic device proper, and formed by a panel in which a display area and a peripheral circuit part for driving the display area are integrally formed in an integrated manner on an insulating substrate, said display device characterized in that:

said panel can switch between an operational mode and a standby mode according to the switching of the side of the electronic device proper between the normal power consumption state and the low power consumption state;

in the operational mode, the panel operates while supplied with the power supply voltage from the side of the electronic device proper, and makes a desired display by driving the display area;

in the standby mode, the panel has standby control means for stopping the driving of the display area and inactivating the circuit part to reduce power consumption of the panel while the panel remains in a state of being supplied with the power supply voltage from the side of the electronic device proper;

said display area comprises pixel electrodes arranged in a form of a matrix, a common electrode opposed to the pixel electrodes, and an electrooptic material retained between the pixel electrodes and the common electrode; and

said circuit part comprises;

a driver for writing a signal voltage to a side of the pixel electrodes according to the display data supplied from the side of the electronic device proper,

a common driver for applying a common voltage to a side of the common electrode,

an offset circuit having a coupling capacitor for generating a predetermined offset voltage to adjust a level of the common voltage with respect to the signal voltage, and

a start circuit for pre-charging the coupling capacitor of the offset circuit to an offset voltage in advance when a return is made from the standby mode to the operational mode, and discharging the coupling capacitor when a transition is made from the operational mode to the standby mode.

The Office Action contends that the phrase within claim 4 of “the electronic device proper” is unclear and confusing (Office Action at page 2).

In response, an applicant for patent is entitled to select the claim language as long as the meaning is reasonably plain and specific. *Ellipse Corporation v. Ford Motor Company*, 312 F.Supp. 646, 660, 164 USPQ 161, 171 (N.D. Ill. 1969).

The plain meaning of claims language is entitled to a strong presumption that it correctly expresses the scope of the claim. *In re Certain Thermometer Sheath Packages*, 205 USPQ 932, 941 (ITC 1979).

In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to *particularly point out and distinctly claim the subject matter which the patentee regards as his*

invention. Texas Digital Systems Inc. v. Telegenix Inc., 308 F.3d 1193, 1201-02, 64 USPQ2d 1812, 1817 (Fed. Cir. 2002).

“For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims.” *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

Practice and procedures found within M.P.E.P. §2173.05(b) provide that:

The fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under 35 U.S.C. 112, second paragraph. *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification.

Here, paragraph [0019] of U.S. Patent Application Publication No. 2006/0181498, the publication document for the above-identified application, provides that:

[0019] FIG. 1 is a block diagram showing a general configuration of a display device according to the present invention. As shown in the figure, the display device 0 is formed in an integrated manner on an insulating substrate 1 formed of glass or the like. A display area 2 is formed at a center of the insulating substrate 1, and a peripheral circuit unit is formed integrally with the display area 2 so as to surround the display area 2. A connection terminal is formed on a top side of the rectangular insulating substrate 1. The connection terminal is connected to a side of an electronic device proper (a set side) via a flexible printed cable (FPC) 11. The FPC 11 is a flat cable of a single-layer structure in which a plurality of wires are arranged in a plane.

Paragraph [0025] of U.S. Patent Application Publication No. 2006/0181498, the publication document for the above-identified application, provides that:

[0025] The DC/DC converter 7 converts a primary power supply voltage supplied from the electronic device proper via the FPC 11 into a secondary power supply voltage in accordance with a specification for the panel (display device 0). The DC/DC converter 7 is used particularly for conversion of a positive-side power supply voltage VDD. On the other hand, the DC/DC converter 7a is used for conversion of a negative-side power supply voltage VSS.

Paragraph [0026] of U.S. Patent Application Publication No. 2006/0181498, the publication document for the above-identified application, provides that:

[0026] The interface 8 including the L/S receives control signals such as a clock signal, a synchronizing signal, an image signal and the like supplied from the set side via the FPC 11. The level shifter L/S shifts levels of the control signals (external control signals) sent from the set side to generate control signals (internal control signals) conforming to specifications for circuit operation within the display device. In the present specification, when the external control signals need to be differentiated from the internal control signals, a number (3) for an external control signal and a number (5) for an internal control signal may be attached following a symbol indicating the type of each control signal. The timing generator 9 processes the clock signal and the synchronizing signal sent from the interface 8 including the L/S to generate, for example, a clock signal necessary for timing control of each circuit part. The analog voltage generator 10 supplies the horizontal driver 4 with analog voltages at a plurality of levels corresponding to gradation levels in advance. The horizontal driver 4 writes the gradated analog signal voltages to the liquid crystal element LC according to image information supplied from the side of the electronic device proper.

Paragraph [0033] of U.S. Patent Application Publication No. 2006/0181498, the publication document for the above-identified application, provides that:

[0033] The display device, which makes a transition to the standby mode in response to the falling of the standby signal STB, has standby control means for stopping the driving of the display area and inactivating the circuit part to reduce panel power consumption while in a state of being supplied with the power supply voltage VDD from the side of *the electronic device proper*. This standby control means is distributed in blocks of the circuit part, and each circuit block performs a control sequence for inactivation in response to the falling of the STB.

Thus, it is believed that the metes and bounds of the phrase within claim 4 of “the electronic device proper” can be readily ascertained.

Withdrawal of the rejections and allowance of the claims is respectfully requested.

Rejections under 35 U.S.C. §103

Paragraph 4 of the Office Action indicates a rejection of claims 1-6 under 35 U.S.C. §103 as allegedly being unpatentable over Applicant’s Admitted Prior Art (AAPA) in view of U.S. Patent Application Publication No. 2001/0035862 to Nakamura et al. (Nakamura).

This rejection is traversed at least for the following reasons.

Claims 1-3 - Claims 2-3 are dependent upon claim 1. Claim 1 is drawn to a display device used as a display part of an electronic device, operating according to display data and power supply voltage supplied from a side of the electronic device proper, and formed by a panel in which a display area and a peripheral circuit part for driving the display area are integrally formed in an integrated manner on an insulating substrate, said display device characterized in that:

said display area comprises pixel electrodes arranged in a form of a matrix, a common electrode opposed to the pixel electrodes, and an electrooptic material retained between the pixel electrodes and the common electrode; and

said circuit part comprises;

a driver for writing a signal voltage to a side of the pixel electrodes according to the display data,

a common driver for applying a common voltage to a side of the common electrode,

an offset circuit having a coupling capacitor for generating a predetermined offset voltage to adjust a level of the common voltage with respect to the signal voltage, and

a start circuit for pre-charging the coupling capacitor of the offset circuit to an offset voltage at a time of a rising edge of the power supply voltage, and discharging the coupling capacitor at a time of a falling edge of the power supply voltage.

Claims 4-6 - Claims 5-6 are dependent upon claim 4. Claim 4 is drawn to a display device used as a display part of an electronic device capable of switching between a normal power consumption state and a low power consumption state, operating according to display data and power supply voltage supplied from a side of the electronic device proper, and formed by a panel in which a display area and a peripheral circuit part for driving the display area are integrally formed in an integrated manner on an insulating substrate, said display device characterized in that:

said panel can switch between an operational mode and a standby mode according to the switching of the side of the electronic device proper between the normal power consumption state and the low power consumption state;

in the operational mode, the panel operates while supplied with the power supply voltage from the side of the electronic device proper, and makes a desired display by driving the display area;

in the standby mode, the panel has standby control means for stopping the driving of the display area and inactivating the circuit part to reduce power consumption of the panel while the panel remains in a state of being supplied with the power supply voltage from the side of the electronic device proper;

said display area comprises pixel electrodes arranged in a form of a matrix, a common electrode opposed to the pixel electrodes, and an electrooptic material retained between the pixel electrodes and the common electrode; and

said circuit part comprises;

a driver for writing a signal voltage to a side of the pixel electrodes according to the display data supplied from the side of the electronic device proper,

a common driver for applying a common voltage to a side of the common electrode,

an offset circuit having a coupling capacitor for generating a predetermined offset voltage to adjust a level of the common voltage with respect to the signal voltage, and

a start circuit for pre-charging the coupling capacitor of the offset circuit to an offset voltage in advance when a return is made from the standby mode to the operational mode, and discharging the coupling capacitor when a transition is made from the operational mode to the standby mode.

Figures 4 and 7 of the specification as originally filed are provided hereinbelow.

FIG. 4

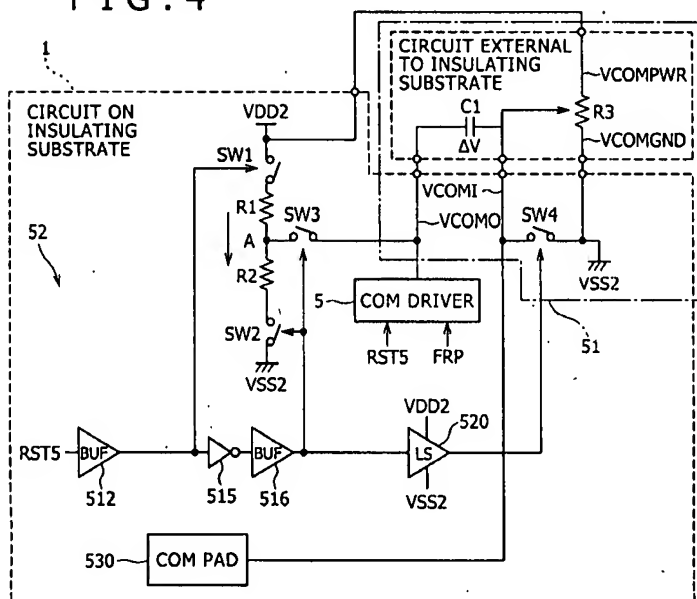
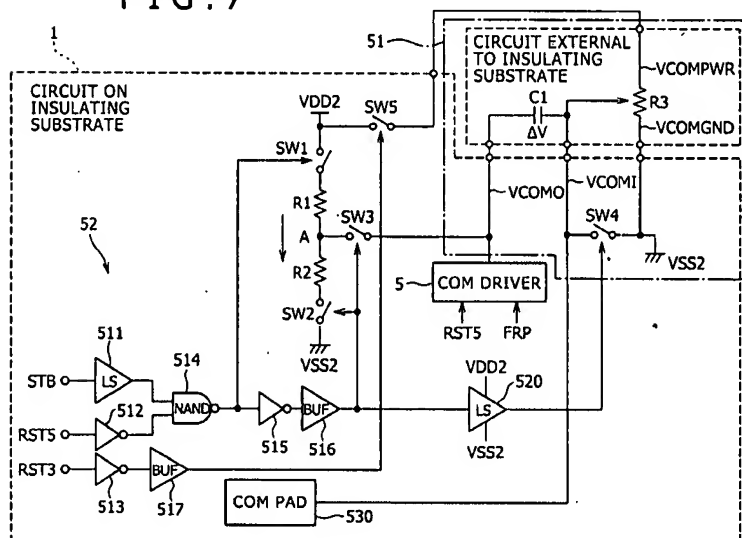


FIG. 7



AAPA - The Office Action readily admits that AAPA fails to disclose, teach, or suggest a start circuit for pre-charging (Office Action at page 3).

- *Thus, AAPA fails to disclose, teach, or suggest a start circuit for pre-charging the coupling capacitor of the offset circuit to an offset voltage in advance when a return is made from the standby mode to the operational mode, and discharging the coupling capacitor when a transition is made from the operational mode to the standby mode.*

Nakamura - The Office Action cites Nakamura for the features that are deficient from within AAPA.

Page 3 of the Office Action cites Figure 10 of Nakamura, which is provided hereinbelow.

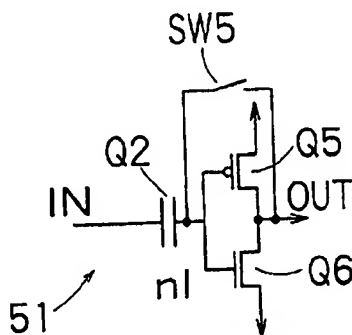


FIG. 10

Paragraph [0132] of Nakamura provides that:

[0132] FIG. 10 is a circuit diagram of the level shifter 51 and FIG. 11 is a waveform diagram of input/output signals to/from the level shifter 51. A thick curve a in FIG. 11 denotes the input signal and a thin curve b indicates the output signal. As shown in

FIG. 10, the level shifter 51 comprises: a capacitor element C1; a PMOS transistor Q5 and an NMOS transistor Q6 constituting an inverter; and an analog switch SW5.

Paragraph [0133] of Nakamura provides that:

[0133] The analog switch SW5 in the level shifter 51 is turned on when the digital pixel data DATA supplied from the graphic controller IC 5 is at the intermediate potential (1.65V) during the blanking period. Consequently, a voltage of one end b of the capacitor element C1 is equivalent to a threshold voltage (about 2.5V) of the inverter and a voltage of $(2.5V - 1.65V =) 0.85V$ is applied across the capacitor element C1.

Paragraph [0134] of Nakamura provides that:

[0134] When the analog switch SW5 is turned off, the digital pixel data DATA supplied from the graphic controller IC 5 is offset-adjusted as much as the voltage of 0.85V across the capacitor element C1, namely, 0.85V, and then transmitted. That is, a voltage fluctuating on the threshold voltage of the inverter vertically as much as only the same level is applied to a gate terminal of each of the PMOS transistor Q5 and the NMOS transistor Q6 constituting the inverter.

Paragraph [0218] of Nakamura provides that:

[0218] For example, in a standby mode of a cellular phone, it is necessary to reduce the power consumption of a display apparatus as much as possible. To reduce the power consumption, it is preferable to reduce the frame frequency. However, when the frame frequency is reduced, flicker stands out conspicuously. Accordingly, it is necessary to perform a process for reducing the number of gray scales of each of RGB to make the flicker inconspicuous. When the frame frequency is lowered, the signal lines can be driven sufficiently on the glass substrate side so long as the amplitude of digital pixel data is reduced.

Nevertheless, Nakamura fails to disclose, teach, or suggest a start circuit for pre-charging the capacitor element C1 to an offset voltage in advance when a return is made from the standby mode to the operational mode, and discharging the capacitor element C1 when a transition is made from the operational mode to the standby mode.

- *Thus, Nakamura fails to disclose, teach, or suggest a start circuit for pre-charging the coupling capacitor of the offset circuit to an offset voltage in advance when a return is made from the standby mode to the operational mode, and discharging the coupling capacitor when a transition is made from the operational mode to the standby mode.*

Withdrawal of this rejection and allowance of the claims is respectfully requested.

Newly added claims

Claims 7-16 - Claims 8-16 are dependent upon claim 7. Claim 7 is drawn to a display device comprising:

a circuit part having a coupling capacitor within an offset circuit and a start circuit,

wherein said coupling capacitor is adapted to generate a predetermined offset voltage to adjust a level of a common voltage with respect to a signal voltage, and

wherein said start circuit is adapted to pre-charge said coupling capacitor to an offset voltage at a time of a rising edge of a power supply voltage, a common voltage from a common driver being applied to said coupling capacitor.

AAPA and Nakamura, either individually or as a whole, fails to disclose, teach, or suggest a display device wherein said start circuit is adapted to pre-charge said coupling capacitor to an offset voltage at a time of a rising edge of a power supply voltage, a common voltage from a common driver being applied to said coupling capacitor.

Allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

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Respectfully submitted,

By 

Ronald P. Kananen

Registration No.: 24,104

Brian K. Dutton

Registration No.: 47,255

RADER, FISHMAN & GRAUER PLLC

Correspondence Customer Number: 23353

Attorneys for Applicant